REMARKS

The claims are claims 1 to 3, 14, 15, 17 and 18.

Claims 1 and 14 are amended. Claims 4 to 13 and 16 are canceled. Claims 1 to 14 were amended to overcome a rejection under 35 U.S.C. 112.

Claims 14, 15, 17 and 18 were objected to for an informality in claim 14. The amendment to claim 14 in response to the rejection under 35 U.S.C. 112 had mooted this objection by canceling the offending phrase.

Claims 1 to 4, 9, 10, 14, 15, 17 and 18 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The Examiner stated that the claims contain subject matter which was not described in the specification. The OFFICE ACTION states at page 3, lines 3 to 9:

> "Applicant sets forth that the invalidate TLB entry command is not issued in response to write transactions (see claim 1, lines 18-19; claim 14, line 14; remarks at page 7, next to last fall paragraph). However, in Applicant's specification, it appears that Applicant discloses issuing an invalidate command in response to a write operation. See paragraph 71 on page 27 of the specification. It is not clear where Applicant has support for not generating an invalidate command in response to a write operation."

The OFFICE ACTION states that this causes the claims to recite subject matter not taught in the application.

Claims 1 and 14 have been amended to delete the recitation of not changing data in any other memory. By these amendments claims 1 and 14 recite subject matter adequately described in the original application.

Claims 1, 3, 9, 10, 14, and 18 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Mason et al

(U.S. Patent No. 5,319,760) and Chang et al (U.S. Patent No. 6,119,204).

Claims 1 and 14 recite subject matter not made obvious by the combination of Mason et al and Chang et al. Claim 1 recites "invalidating a portion of the plurality of translated memory address in the TLB in a manner that is qualified by the shared indicator in response to an invalidate TLB entry command issued from the processor." Claim 14 recites "the control circuitry is responsive to an invalidate TLB entry command to invalidate entries within said storage circuitry qualified by the shared indicator field." The OFFICE ACTION notes the "address space match" bit disclosed in Mason et al ad making obvious the claimed shared indicator. The Applicant respectfully submits that Mason et al fails to teach that a cache invalidation action can be "qualified" by this "address space match" bit. Mason et al states at column 10, lines 7 to 11:

> "If the address space match field (bit <4>, Table A) is clear (zero), the current ASN and the field 94 must match for the PTE to be used, but if set (logic one) then there need not be a match, i.e., the address space numbers are ignored."

The Applicant respectfully submits this teaching of Mason et al indicates that the address match field controls whether address space number is used in determining whether that tag provides a match. Thus the operation is conditioned on the address space number and not on the address space match bit. Mason et al states at column 9, lines 51 to 68 (just before the above quoted portion):

> "Referring to FIG. 10, the virtual address 76 on the bus 56 (seen in FIG. 8) is used to search for tag match for a PTE in the translation buffer, and, if not found, then Seg1 field 78 is used to index into a first page table 85 found at a base address stored in an internal register 86 referred to as the page table base register. The entry 87 found at the Seg1 index

> in table 85 is the base address for a second page table 88, for which the Seg2 field 79 is used to index to an entry 89. The entry 89 points to the base of a third page table 90, and Seg3 field 80 is used to index to a PTE 91. The physical page frame number from PTE 91 is combined with the byte offset 77 from the virtual address, in adder 92, to produce the physical address on bus 54. As mentioned above, the size of the page mapped by a PTE, along with size of the byte offset 77, can vary depending upon the granularity hint."

The Applicant respectfully submits that this teaching of Mason et al provides a strong implication that the conditional match based on the address space match bit described in the following lines in column 10 takes place in the normal operation of the translation buffer. Neither paragraph includes any teaching about using the address space match bit in determining whether to invalidate an entry as recited in claims 1 and 14. Accordingly, claims 1 and 14 are allowable over the combination of Mason et al and Chang et al.

Claims 3 and 18 recite subject matter not made obvious by the combination of Mason et al and Chang et al. Claim 3 recites "invalidating a translated memory address in the TLB only if the corresponding task identification value indicates the program task identified by said invalidate task TLB entry except shared command and the corresponding shared indicator indicates the translated memory address is not shared by more than one of the plurality of program tasks." Claim 18 recites the control circuitry operates "to invalidate a translated memory address in the storage circuitry only if the corresponding task identification value corresponds to said task identification value of said invalidate task TLB entry except shared command and the corresponding shared indicator indicates the translated memory address is not shared." The OFFICE ACTION states at page 5, lines 14 to 18:

> "As per claims 3 and 18, Mason et al. teaches invalidating entries in the TB that match a particular address space number, where addresses that do not match the address space

number are not flushed from the TB. See column 11, lines 57-61. Therefore, the combination of Mason et al. and Chang et al. teaches invalidating entries using an invalidation command where the address space number in the TB matches the address space number of the invalidate operation."

Mason et al states at column 11, line 57 to column 12, line 3 (including the portion cited in the OFFICE ACTION):

> "The architecture as described above allows a processor to implement address space numbers (process tags) to reduce the need for invalidation of cached address translations in the translation buffer for process-specific addresses when a context switch occurs. The address space number for the current process is loaded by a privileged instruction from field 103 into an internal processor register 95.
>
> "In the page table entry 81 of FIG. 9 and Table A, there is a field (bit <4>) called 'address space match.' This feature allows an operating system to designate locations in the system's virtual address space 97 which are shared among all processes. Such a virtual address refers to the same physical address in each process's address space."

This portion of Mason et al teaches that an invalidation command directed to the translation buffer may be limited to a particular address space number. The Applicant respectfully submits that the "only if" language of claims 3 and 18 is not made obvious by Mason et al. In accordance with the teachings of Mason et al at, if the address space match indicates a shared address space, then the command need not match the address space number. Thus a translation buffer entry having a different address space number and an address space match bit indicating shared memory would also be invalidated. This is contrary to the "only if" language of claims 3 and 18. Accordingly, claims 3 and 18 are not made obvious by the combination of Mason et al and Chang et al.

Claims 2 and 17 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Mason et al (U.S. Patent No.

5,319,760), Chang et al (U.S. Patent No. 6,119,204) and Bausch (U.S. Patent No. 6,339,816).

Claims 2 and 17 recite subject matter not made obvious by the combination of Mason et al, Chang et al and Bausch. Claim 2 recites "invalidating a translated memory address in the TLB only if the corresponding shared indicator indicates the translated memory address is shared by more than one of the plurality of program tasks." Claim 17 recites the control circuitry operates "to invalidate a translated memory address in the storage circuitry only if the corresponding shared indicator indicates the translated memory address is shared by more than one of the plurality of program tasks." The Applicant respectfully submits that the "only if" language of claims 2 and 17 is not made obvious by Mason et al. Mason et al teaches an address space match bit that enables a match even if the address space number does not match. However, Mason et al does not teach only a match is precluded if the address space number of the translation buffer matches the request and the address space match bit requires an address space number match. Mason et al states at column 13, lines 5 to 15:

> "In order to enforce the memory isolation requirements, the TB must be completely flushed whenever (1) there are any entries in the TB that have the match field (bit <4>) indicating match all, and (2) any of the following events occurs: (a) the currently executing entity on the real machine changes from one VM to another VM, (b) the currently executing entity on the real machine changes from some VM to the VMM, or (c) the currently executing entity on the real machine changes from the VMM to any VM."

The conditions of (2) are context switches. Note that this teaching requires the whole translation buffer to be flushed if "there are any entries in the TB that have the match field (bit <4>) indicating match all." This portion requires invalidation of more of the translation buffer than recited in claims 2 and 17 and

thus fails to make obvious the "only if" language of these claims. Mason et al at column 13, line 24 to column 14, line 6 includes an alternative embodiment that includes an additional "disable match" CPU state that can be used to enable or disable the address space match bit. As shown in the table bridging columns 13 and 14, there are match cases when the address space match bit is in either state. Thus this fails to teach the "only if" limitation of claims 2 and 17. Accordingly, claims 2 and 17 are not made obvious by the combination of Mason et al, Chang et al and Bausch.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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